a checker coupled to the output of the multiplexer to determine whether an instruction has executed properly;

a replay queue to temporarily store instructions, an output of the replay queue coupled to a second input of the multiplexer; and

a controller coupled to the checker to determine when to load an instruction into the replay queue and to determine when to unload the replay queue.

10. (Original): The processor of claim 9 and further comprising a staging section coupled between the checker and a third input to the multiplexer to provide a replay loop, the controller controlling the multiplexer to select either the output of the scheduler, the replay loop or the output of the replay queue.

11. (Original): The processor of claim 9 wherein the controller loads an instruction into the replay queue when the instruction is not ready to execute properly, and unloads the instruction from the replay queue when the instruction is ready to execute properly.

12. (Original): The processor of claim 9 wherein the controller determines when to unload the replay queue based on a data return signal.

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13–~~20~~ 19. (Previously Canceled)

20. ~~21~~. (New): The processor of claim 4, wherein if said long latency instruction is ready for execution, the long latency instruction is unloaded from the replay queue.

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21 ~~22.~~ (New): The processor of claim 5, wherein a controller determines whether to unload the replay queue based on a data return signal.

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22. ~~23.~~ (New): The processor of claim 6 wherein a controller determines whether to unload the replay queue based on a data return signal.

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